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Reliability characterization of SiON and MGHK MOSFETs using flicker noise and its correlation with the bias temperature instability

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ABSTRACT

Bias temperature instability (BTI) is one of the critical device degradation mechanisms in poly-Si/SiON and metal gate/high-*k* complementary metal-oxide-semiconductor (CMOS) technologies. Using the pre- and post-BTI flicker noise measurements, we investigated the bulk trap density, N_t, in both of these technologies. The low-frequency noise spectra were predominantly of $1/f^{\gamma}$ type with $\gamma < 1$ for NMOS and $\sim$1 for PMOS. For SiON based technologies, the lower V_{TH} degradation due to PBTI was noticed while considerable V_{TH} degradation was observed for NBTI in both SiON and MGHK technologies. Both MGHK and SiON pFETs show a clear increase in the effective volume trap density, N_t, after NBTI. The increase in N_t in MGHK n-MOSFETs during PBTI is markedly higher than that in MGHK p-MOSFETs during NBTI.

1. Introduction

In downscaled CMOS devices, the use of SiO_2 as a gate dielectric has reached physical limits due to the high leakage currents [1]. The high-*k* alternatives for SiO_2 include HfO_2 [2]. However, reliability problems relating to the intrinsic material quality of these dielectrics still exist [1,3–5]. Fluctuations in the channel current are governed by carrier trapping and de-trapping within a few nm from the Si interface [6–7]. As a result, the low-frequency noise has been used as a diagnostic tool for understanding processes and mechanisms affecting device reliability. The low-frequency noise also constitutes a critical technology parameter [8–9]. It can be used to determine the effectiveness of the gate stack when the sources of the current fluctuations are charge trapping – de-trapping events [10–14]. The noise investigations in the past have been focused on the effects of various processing parameters such as the deposition technique, HfO_2 thickness, interfacial layer and type of metal gate on 1/f noise [15–21]. Various fluctuation processes can be responsible for the 1/f noise in different materials and devices. For this reason, practical applications of new material systems usually require a thorough investigation of the specific features of the low-frequency noise in the material, and development of methods for its reduction [22–26].

The bias temperature instability (BTI) is one of the important degradation mechanisms in the metal gate high-*k* and poly-Si/SiON CMOS technologies and has been studied extensively in the past [27–33]. The bias temperature dependent instability in transistors causes an increase in the threshold voltage of the MOSFET when the device is stressed at higher voltage and high temperature. The threshold voltage shift consequently leads to a decrease in the drain current, which results in the reduced lifetime [34–36]. Flicker noise can be used to investigate newly generated traps as a result of electrical stressing through BTI. In addition, it can be used to investigate dielectric trap distribution and characteristics by utilizing measurements both before and after this stressing.

In this work, we investigate the effect of the BTI stress on n- and p-channel MOSFETs with [i] HfO_2 gate oxide and TaN as gate material (MGHK) as well as [ii] SiON dielectric layer with poly-Si gate material (SiON) by using flicker (1/f) noise measurements. The pre and post BTI effective dielectric volume trap density (N_t) is also evaluated.

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2. Experimental

The devices used for this study consisted of SiON and metal gate/high-k (MGHK) n- and p-MOSFETs of nominal length with area of 0.06–0.09 μm^2. The ratio of the equivalent oxide thickness (EOT) for MGHK to SiON devices was 0.56. The on-wafer noise measurements were carried out in the linear regime at the constant drain voltage $|V_{DS}| = 0.05$ V and the constant drain current values using BTA9812 noise analyzer system in conjunction with NoisePro software from Proplus. Flicker noise on each tested device was measured at three different values of the drain current, I_D, corresponding to 10 μA, 100 μA and 170 μA. The charge-pumping measurements were performed on comparable samples by measuring the substrate current while simultaneously applying the voltage pulses of fixed amplitude, rise time, fall time and frequency to the gate.

The BTI stress was applied at a temperature of 125 °C for three different constant voltage stress values: V_{G1}, V_{G2}, and V_{G3} (where $V_{G3} > V_{G2} > V_{G1}$) applied to n- and p-MOSFET samples. Four devices under test (DUTs) were measured at each voltage condition. The absolute shift in threshold voltage, ΔV_{TH}, was determined at regular intervals, up to the stress time of about 1000 s. All post-stress flicker noise measurements were carried out after a considerable amount of recovery time spanning a number of days.

3. Results and discussion

Fig. 1 shows the normalized I_D-V_G characteristics of MGHK and SiON n- and p-MOSFETs. The tested SiON and MGHK n-MOSFETs show a comparable drive current, I_D. A similar observation is made for SiON and MGHK p-MOSFETs. Fig. 2 shows the low-frequency (LF) drain current noise spectra (S_{ID}) comparison of MGHK and SiON n-MOSFETs while Fig. 3 presents the comparison for MGHK and SiON p-MOSFETs. The data are the average values of the current spectral density, S_{ID}, for multiple samples measured at three different drain currents I_D. Fitting is carried out at the $V_G \sim V_{TH}$ condition, which corresponds to the drain current $I_D = 10$ μA. For SiON and MGHK MOSFETs, the LF noise spectra follow $1/f^{\gamma}$ type dependence, where p-MOSFETs have $\gamma \sim 1.04$–1.09. It has been established in prior studies that when $\gamma \sim 1$, the traps are evenly distributed through the tunneling distance and the energy band gap [37,38]. The tested SiON and MGHK n-MOSFETs reveal $\gamma \sim 0.83$, which suggests that there is a larger number of higher

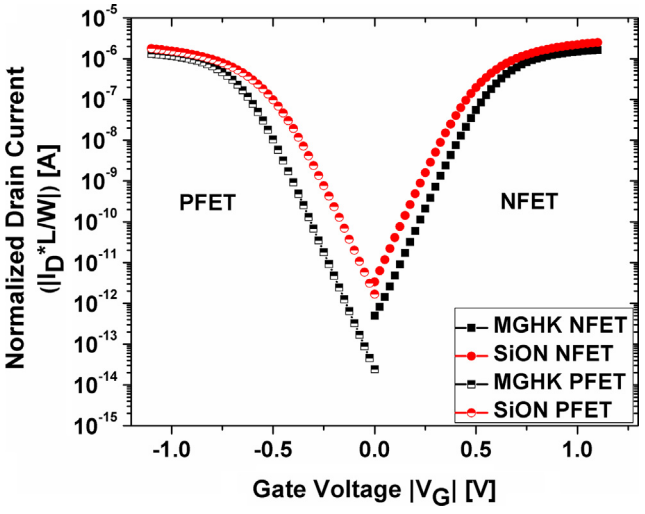

Fig. 1. Normalized drain current versus gate voltage characteristics with $V_{DS} = 0.05$ V for MGHK and SiON n- and p-MOSFETs.

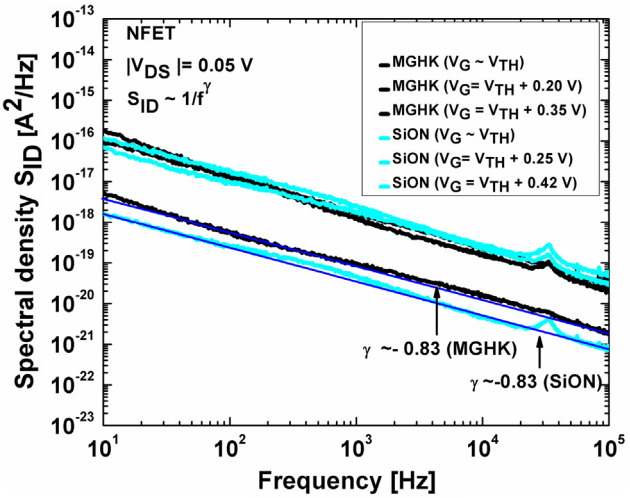

Fig. 2. Low-frequency noise spectra at $|V_{DS}| = 0.05$ V for both SiON and MGHK n-MOSFETs. Shown are average values of S_{ID} (drain current noise spectral density for multiple samples at different drain currents. The allometric fitting shown is done for both SiON and MGHK p-MOSFETs at V_{TH} condition ($V_G \sim V_{TH}$).

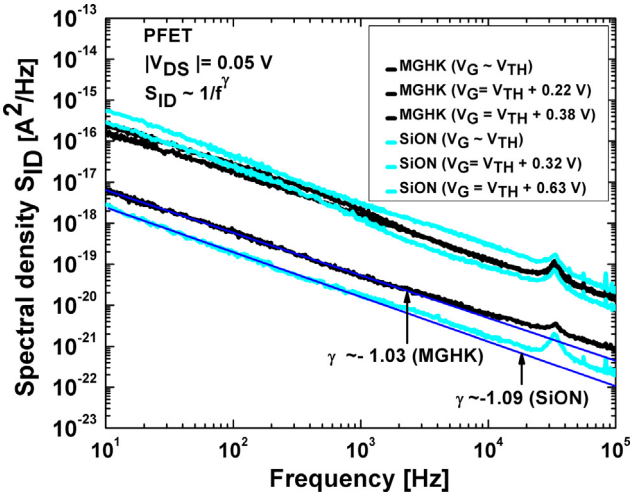

Fig. 3. Low-frequency noise spectra at $|V_{DS}| = 0.05$ V for both SiON and MGHK p-MOSFETs. Shown are average values of S_{ID} (drain current noise spectral density) for multiple samples at different drain currents. The fitting is performed for both SiON and MGHK p-MOSFETs at V_{TH} condition ($V_G \sim V_{TH}$).

frequency traps, and the distribution of these traps are skewed closer to the dielectric interface [37,38]. Fig. 4 shows the average low-frequency noise values for multiple samples at f = 25 versus the drain current (I_D) that they were measured at. This allows us to see the transition from weak to moderate/strong inversion. Noise levels were seen to be similar for SiON and MGHK n-MOSFETs at every drain current I_D. The same can be seen for SiON and MGHK p-MOSFETs.

Assuming a trapping origin of 1/f noise, the effective volume trap density, N_t, can be estimated from the input-referred noise spectral density, S_{VG} (S_{ID}/G_m^2), using the formula

$$S_{VFB} = \frac{q^2 kTN_t}{WLC_{inv}^2 \alpha_t f}, \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, C_{inv} is the inversion capacitance per unit area given by $C_{inv} = \varepsilon_{ox}.\varepsilon_A/t_{inv}$, ε_{ox} is the permittivity of SiO_2, α_t is the tun-

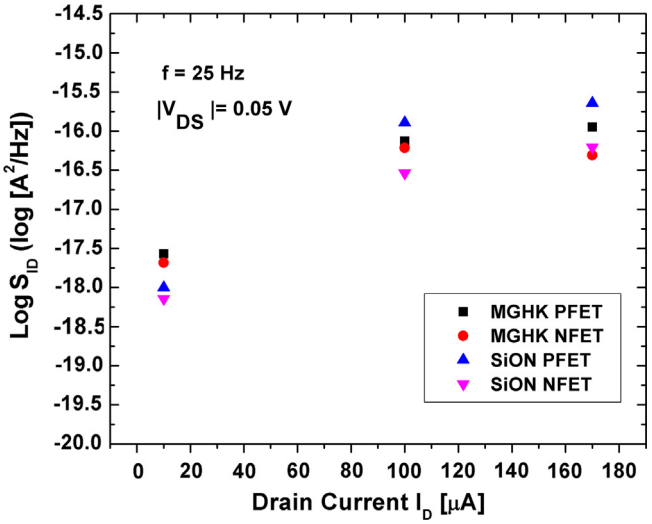

Fig. 4. Drain current noise versus drain current characteristics for MGHK and SiON n- and p-MOSFETs.

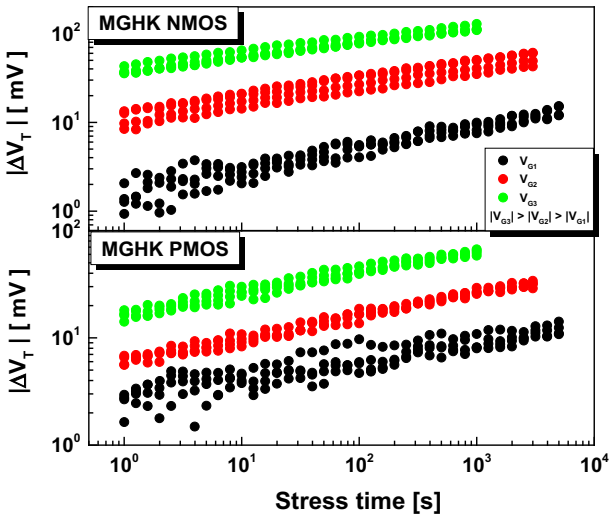

Fig. 5. ΔV_{TH} versus stress time at 125 °C for various stress voltages showing V_{TH} degradation in MGHK n- and p-MOSFETs. There is a clear correlation between applied stress and ΔV_{TH} for both PBTI and NBTI.

neling parameter and f is the frequency [39–40]. The surface trap density, D_t, was estimated as

$$D_t = 4kTzN_t, \quad (2)$$

where z is the tunneling distance of the carrier from the Si/high-*k* interface. It is evaluated at f = 25 Hz to be 1.49 nm for SiON and 2.08 nm for MGHK MOSFETs, respectively and was calculated using the formula

$$\frac{1}{2\Pi f} = \tau_o \exp(\alpha_t z). \quad (3)$$

The value of the tunneling parameter α_t was 1.2×10^8 cm^{-1} and 0.86×10^8 cm^{-1} for SiON and MGHK MOSFETs, respectively. The calculated noise parameters are shown in Table 1 while the final calculated values of N_t and D_t are indicated in Table 3. The charge pumping measurements were performed on comparable samples to estimate the interface state density, N_{it}, using the formula

$$N_{it} = I_{cp}/qfA, \quad (4)$$

where I_{cp} is the charge pumping current, f is the test frequency, and A is the channel area (in cm^2 units) [41]. The calculated interface state density, N_{it}, was found to be comparable to the previously calculated pre-stress surface trap density values, D_t, that were extracted from the flicker noise measurements, as shown in Table 3.

Fig. 5 presents the absolute threshold voltage shift for MGHK n- and p-MOSFETs, respectively, at 125 °C under different stress conditions. Both, negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI), show a clear increase in the absolute threshold voltage V_{TH}. Table 2 shows the ΔV_{TH} for both MGHK and SiON MOSFETs under different stress conditions from V_{G1} to V_{G3} where $V_{G3} > V_{G2} > V_{G1}$. The V_{TH} shift dependents on both the applied stress magnitude and the stress time. The spot values of ΔV_{TH} at the stress time ~1000 s along the fitted curves show considerable ΔV_{TH} shift for MGHK n- and p-MOSFETs. It can be seen that PBTI ΔV_{TH} is much higher at each applied stress value, and it peaks at ~100 mV at the applied stress voltage of V_{G3}. The NBTI ΔV_{TH} peaks at ~65 mV at the same applied stress voltage.

Fig. 6 shows the absolute threshold voltage shift for SiON n- and p-MOSFETs at 125 °C under different stress conditions and different time intervals. Unlike the MGHK type devices where both n- and p- type devices show clear threshold voltage shift, only SiON p-MOSFETs under NBTI were observed to have significant ΔV_{TH} at three different applied stress conditions, reaching a peak of ~32 mV at stress time ~1000 s and under an applied stress corresponding to V_{G3}. PBTI reveals lower ΔV_{TH} degradation.

The flicker noise measurements for post-BTI devices can be used to investigate newly generated traps [42]. Fig. 7 and Fig. 8 present the pre- and post-BTI low-frequency noise spectra for n- and p-type MGHK and SiON MOSFETs for a given voltage V_{G1} after 1000 s stress respectively. In all cases, a slight increase in the newly generated traps is observed post-stress except for the SiON p-MOSFET where a larger increase observed, leading to the increased drain current noise spectral density after the stress. The effective volume trap density post-BTI at 25 Hz for devices stressed to V_{G3} is calculated following the method described earlier. It is compared to the N_t value determined pre-BTI. The pre- and post-stress results are shown in Table 3.

From Table 3, one can see that the MGHK PBTI reveal a larger increase in N_t than NBTI. The data indicate that MGHK n- and p-MOSFETs have the increased density of interface traps as a result of the electrical stressing. The latter explains the appearance of the generation-recombination humps in the post-BTI spectra as the capture and emission of carriers through these newly generated traps causes fluctuations in the number of free carriers. The trapped charge can also cause fluctuations in the mobility, electric field and barrier height.

A comparison of the extracted N_t post-BTI in SiON MOSFETs (Table 3), calculated at f = 25 Hz, indicate that NBTI creates higher density of interface traps compared to PBTI. The shift ΔV_{TH} for NBTI in SiON MOSFETs is comparable to conventional MGHK devices. However, SiON devices under PBTI show the lower threshold voltage shifts, close to the operation condition. The exception is the high-voltage stress, close to the dielectric breakdown, at which point the instability can be observed at shorter stress times [34].

Table 1
Noise parameters: values at $V_G \sim V_{TH}$, |Vds| = 0.05 V, Freq = 25 Hz.

	S_{VG} (V^2/Hz)	Z (nm)	α_t (1/cm)	C_{inv} (F/cm^2)
N-MGHK	1.39×10^{-10}	2.08	0.86×10^8	2.59×10^{-6}
P-MGHK	1.18×10^{-10}	2.08	0.86×10^8	2.55×10^{-6}
N-SiON	9.99×10^{-11}	1.49	1.2×10^8	1.56×10^{-6}
P-SiON	2.38×10^{-10}	1.49	1.2×10^8	1.44×10^{-6}

Table 2
ΔV_{TH} at 1000 s (milli-volts).

Applied V_G (V)	N-MOSFET		P-MOSFET	
	MGHK	SiON	MGHK	SiON
V_{G1}	~10	~3	~8	~12
V_{G2}	~40	~3	~30	~20
V_{G3}	~100	~4	~65	~32

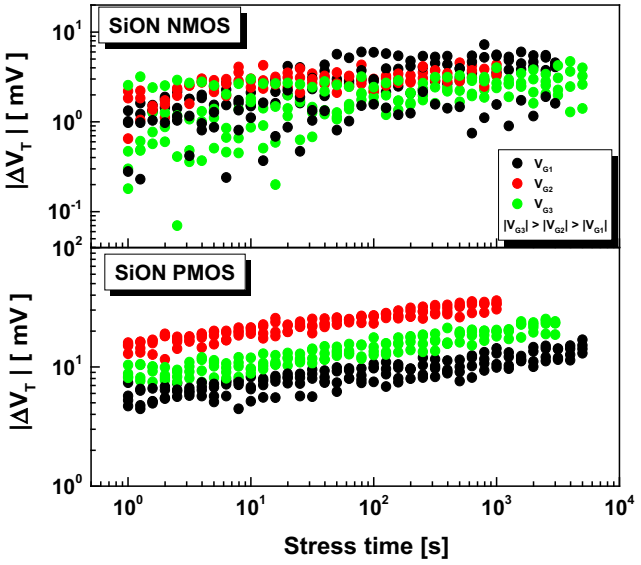

Fig. 6. ΔV_{TH} versus stress time at 125 °C for various stress voltages showing V_{TH} degradation on SiON n- and p-MOSFETs. PBTI for these devices is not seen to cause any clear or significant ΔV_{TH}. There is a clear correlation between applied stress and ΔV_{TH} for NBTI.

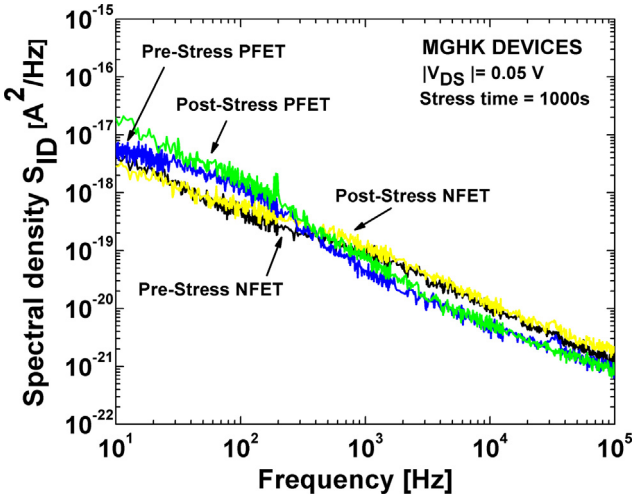

Fig. 7. Pre- and Post-BTI low-frequency noise spectra at $|V_{DS}| = 0.05$ V for n- and p-MGHK MOSFETs. Post-stress values shown are for V_{G3} after 1000 s.

This effect can be attributed to the bulk defect generation in the gate oxide.

The absolute threshold voltage ΔV_{TH} of the MOSFET increases while the device is biased in the inversion mode [34]. There are distinct differences in the physical degradation mechanisms between PBTI and NBTI due to the defect structure of the dielectrics, asymmetry in the band structures of the Si/high-*k*/metal gate stack and the opposite polarity of the gate bias [34]. During NBTI in p-MOSFETs, hole trapping and interface state generation have been observed [36] with the physical degradation process involving hole trapping in the dielectric layer and interface-state generation at the interface for both MGHK and SiON MOSFETs. The basic degradation mechanism for both MGHK and SiON MOSFETs is similar. The positive charges can be trapped at interface and near-interface states (border traps), as well as in the bulk of the oxide. The trapped charges, which are very close to the inversion layer, lead to degradation in the channel carrier mobility due to Coulomb scattering effect. As a result of the mobility degradation, the peak transconductance of both MGHK and SiON devices in the linear regime decrease with increasing voltage shift. This would explain why both MGHK and SiON p-MOSFETs show an increase in effective dielectric volume trap density N_t after NBTI.

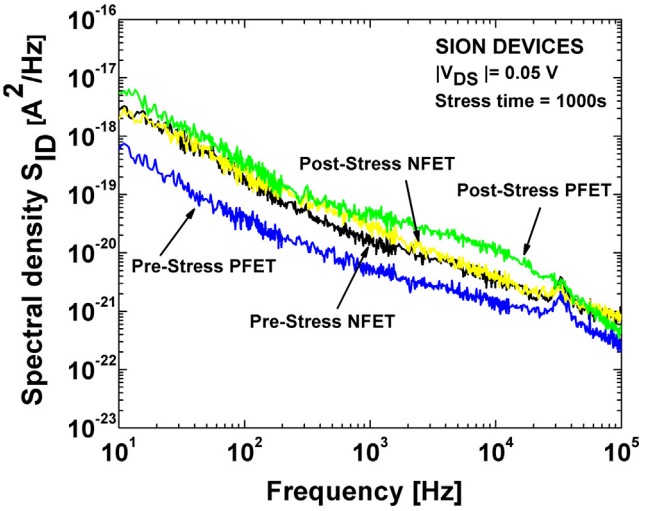

Fig. 8. Pre- and Post-BTI low-frequency noise spectra at $|V_{DS}| = 0.05$ V for n- and p-MGHK MOSFETs. Post-stress values shown are for V_{G3} after 1000 s. Note the enhanced S_{ID} change during BTI in p-MOSFETs as opposed to n-MOSFETs.

Table 3
Pre and post stress results.

	P-MGHK	N-MGHK	P-SiON	N-SiON
Pre-stress				
N_t (1/cm^3)	1.34×10^{18}	8.17×10^{17}	4.87×10^{17}	2.80×10^{17}
D_t (1/cm^2)	2.93×10^{10}	1.77×10^{10}	7.59×10^{9}	4.37×10^{9}
Post-stress				
N_t (1/cm^3)	1.49×10^{18}	1.80×10^{18}	2.02×10^{18}	9.93×10^{17}
D_t (1/cm^2)	3.25×10^{10}	3.93×10^{10}	3.14×10^{10}	1.54×10^{10}

On the other hand, during PBTI on n-MOSFETs, MGHK devices show electron trapping in the high-*k* layer and/or the region between the high-*k* layer and the interfacial oxide layer [43] while electron trapping is seen to be small or negligible in SiON devices. For this reason, we see an increase in N_t in MGHK n-MOSFETs during PBTI that is markedly higher than the increase of N_t in SiON n-MOSFETs. The degradation features vary for NBTI and PBTI due to difference in the charge location [36]. The Coulomb scattering is generally weaker since trapped charge is separated from the inversion channel by the interfacial oxide layer [36]. This means that the channel carrier mobility remains constant, independent of the amount of trapped charge. For this reason, the transistor characteristic is only horizontally shifted on the voltage scale.

4. Conclusions

In this work, the flicker noise measurements were used as the diagnostic tool for understanding MGHK and SiON MOSFETs in terms of the correlation between bulk trapping density ($N_{t)}$ and BTI. The increase in N_t was seen in all cases after electrical stressing with a larger increase seen with PBTI as compared to NBTI in MGHK devices. A symmetric trap distribution was observed for MGHK and SiON p-MOSFETs while the tested n-MOSFETs exhibited an asymmetric trap distribution. An analysis of the threshold voltage shift ΔV_{TH} of the different types of MOSFETs under BTI was performed. Both n- and p- type devices show clear threshold voltage shift under BTI while only SiON p-MOSFETs under NBTI were observed to have significant threshold voltage shift at applied stress conditions. Finally, a comparison between the physical degradation mechanisms in these MOSFETs was used to explain calculated values of N_t.

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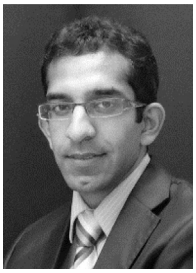
References

[1] Kingon AI, Maria JP, Streiffer SK. Alternative dielectrics to silicon dioxide for memory and logic devices. Nature 2000;406:1032–8.
[2] Wilk GD, Wallace RM, Anthony JM. High-k gate dielectrics: current status and materials properties considerations. J Appl Phys 2001;89(10):5243–75.
[3] Groeseneken G, Pantisano L, Ragnarsson L-Å, Degraeve R, Houssa M, Kauerauf T, et al. Achievements and challenges for the electrical performance of MOSFET's with high-k gate dielectrics. In: Proc. Physical and Failure Analysis of Integrated Circuits (IPFA), Hsinchu, Taiwan, R.O.C.; 2004. p. 147–55.
[4] Carter RJ, Cartier E, Kerber A, Pantisano L, Schram T, De Gendt S, et al. Passivation and interface density of SiO_2/ HfO_2 based/polycrystalline-Si gate stacks. Appl Phys Lett July 2003;83:533–5.
[5] Young EWA. The high k challenges in CMOS advanced gate dielectric process integration. In: Huff HR, Fabry L, Kishino S, editors. Proc. Semiconductor Silicon, Pennington, NJ; 2002. p. 735–46.
[6] Simoen E, Claeys C. Chapter 8. In: Balandin A, editor. Noise and fluctuations control in electronic devices. Los Angeles: Amer Scientific Pub; 2002.
[7] Simoen E, Mercha A, Claeys C. What can low-frequency noise learn us about the quality of thin-gate dielectrics. In: Sah CT, Sundaram KB, Deen MJ, Landheer D, Brown WD, Misra D, editors. Proc. silicon nitride. Pennington (NJ): Amer Scientific Pub; 2003. p. 153 [2002].
[8] Simoen E, Claeys C. On the flicker noise in submicron silicon MOSFETs. Solid-State Electron 1999;43:865–82.
[9] Claeys C, Simoen E, Mercha A. Low frequency noise assessment of silicon substrates and process modules for deep submicron CMOS technology nodes. J Electrochem Soc 2004;151(5):G307–18.
[10] Kapila G, Goyal N, Maheta VD, Olsen C, Ahmed K, Mahapatra S. A comprehensive study of flicker noise in plasma nitrided SiON p-MOSFETs: process dependence of pre-existing and nbti stress generated trap distribution profiles. In: Proc. IEDM; 2008. p. 103–6.
[11] Yasuda Y, Liu T-JK, Hu CM. Flicker-noise impact on scaling of mixed-signal CMOS with HfSiON. IEEE Trans Electr Dev 2008;55(1):417–22.
[12] Magnone P, Crupi F, Pantisano L, Pace C. Fermi-level pinning at polycrystalline silicon-HfO 2 interface as a source of drain and gate current 1/f noise. Appl Phys Lett 2007;90:073507.
[13] Morshed T, Devireddy SP, Rahman MS, et al. A new model for 1/f noise in high-k MOSFETsk. In: Proc. IEDM; 2008. p. 561–64.
[14] Kaczer B, Grasser T, Martin-Martinez J, Simoen E, Aoulaiche M, Roussel Ph.J. NBTI from the perspective of defect states with widely distributed time scales. In: Proc. IRPS; 2009. p. 55–60.
[15] Claeys C, Simoen E, Mercha A, Pantisano L, Young EJ. Lowfrequency noise performance of HfO_2-based gate stacks. J Electrochem Soc 2005;152(9): F115–23.
[16] Simoen E, Mercha A, Pantisano L, Claeys C, Young E. Low-frequency noise behavior of SiO_2-HfO_2 dual-layer gate dielectric nMOSFETs with different interfacial thickness. IEEE Trans Electron Dev 2004;51(5):780–4.
[17] Simoen E, Mercha A, Claeys C, Young E. Correlation between the 1/f noise parameters and the effective low-field mobility in HfO_2 gate dielectric n-channel metal–oxide–semiconductor field-effect transistors. Appl Phys Lett 2004;85(6):1057–9.
[18] Simoen E, Mercha A, Pantisano L, Claeys C, Young E. Tunneling 1/fγ noise in 5 nm HfO_2/2.1 nm SiO_2 gate stack n-MOSFETs. Solid State Electron May 2005;49(5):702–7.
[19] Srinivasan P et al. Gate electrode effects on low-frequency (1/f) noise in p-MOSFETs with high-κ dielectrics. Solid State Electron. Jun. 2006;50(6):992–8.
[20] Srinivasan P, Simoen E, Pantisano L, Claeys C, Misra D. Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs. Microelectron Eng 2005;80:226–9.
[21] Srinivasan P, Simoen E, De Jaeger B, Claeys C, Misra D. 1/f noise performance of MOSFETs with HfO_2 and metal gate on Ge-onInsulator substrates. In: Proc. E-MRS, symp. Germanium-based semicond. from mater devices, Spring; 2006.
[22] Balandin AA. Low-frequency 1/f noise in graphene devices. Nat Nanotechnol 2013;8:549–55.
[23] Renteria J, Samnakay R, Rumyantsev SL, Jiang C, Goli P, Shur MS. Low-frequency 1/f noise in MoS2 transistors: relative contributions of the channel and contacts. Appl Phys Lett 2014;104(15):153104-1–4-5.
[24] Rumyantsev SL, Jiang C, Samnakay R, Shur MS, Balandin A. 1/f noise characteristics of MoS2 thin-film transistors: comparison of single and multilayer structures. IEEE Electron Device Lett 2015;36(5):517–9.
[25] Balandin A, Cai S, Li R, Wang KL, Rao VR, Viswanathan CR. Flicker noise in GaN/$Al_{0.15}Ga_{0.85}$ N doped channel heterostructure field effect transistors. IEEE Electron Device Lett 1998;19(12):475–7.
[26] Balandin A, Morozov SV, Cai S, Li R, Wang KL, Wigeratne G, et al. Low flicker-noise GaN/AlGaN heterostructure field-effect transistors for microwave communications. IEEE Trans Microwave Theory Tech 1999;47(8):1413–7.
[27] Islam AE, Kufluoglu H, Varghese D, Mahapatra S, Alam MA. Recent Issues in negative-bias temperature instability: initial degradation field dependence of interface trap generation hole trapping effects and relaxation. IEEE Trans Electr Dev 2007;54(9):2143–54.
[28] Grasser T, Wagner P-J, Hehenberger Ph, Goes W, Kaczer B. A rigorous study of measurement techniques for negative bias temperature instability. IEEE Trans Dev Mater Rel 2008;8(3):526–35.
[29] Mahapatra S, Alam MA. Defect generation in p-MOSFETs under negative-bias stress: an experimental perspective. IEEE Trans Dev Mater Rel 2008;8(1):35–46.
[30] Bersuker G, Sim JH, Park CS, Young CD, Nadkarni SV, Choi R, et al. Mechanism of electron trapping and characteristics of traps in HfO_2 gate stacks. IEEE Trans Dev Mater Rel 2007;7(1):138–45.
[31] Sato M, Umezawa N, Shimokawa J, et al. Physical model of the PBTI and TDDB of la incorporated HfSiON gate dielectrics with pre-existing and stress-induced defects. In: Proc. IEDM; 2008. p. 119–22.
[32] Ioannou DP, Mittl S, Rosa GL. Positive bias temperature instability effects in nMOSFETs with TiN gate stacks. IEEE Trans Dev Mat Rel 2009;9(2):128–34.
[33] Cartier E, Kerber A. Stress-induced leakage current and defect generation in nFETs with TiN gate stacks during positive-bias temperature stress. In: Proc. IRPS; 2009. p. 486–92.
[34] Kerber A, Cartier E. Bias temperature instability characterization methods. In: Grasser T, editor. Bias temperature instability for devices and circuits. London (UK): Springer-Verlag; 2013. p. 3–31.
[35] Stathis JH, Zafar S. The negative bias temperature instability in MOS devices: a review. Microelectron Reliab 2006;46(2–4):270–86.
[36] Schroder D, Babcock JF. Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing. J Appl Phys 2003;94:1–18.
[37] Christensson S, Lundstrom I, Svensson C. Low frequency noise in MOS transistors-I. theory. Solid-State Electron 1968;11:797.
[38] Surya C, Hsiang TY. Theory and experiment on the 1/f' noise in p-channel metal-oxide-semiconductor field-effect transistors at low drain bias. Phys Rev 1986;33(7):4498.
[39] Ghibaudo G, Roux O, Nguyen-Duc C, Balestra F, Brini J. Improved analysis of low frequency noise in field-effect MOS transistors. Phys Status Solidi A 1991;124(2):571–81.
[40] Hung KK, Ko PK, Hu C, Cheng YC. A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. IEEE Trans Electron Devices Mar 1990;37(3):654–65.
[41] Paulsen RE, White MH. Theory and application of charge pumping for the characterization of Si-SiO_2 interface and near-interface oxide traps. IEEE Trans Electron Devices 1994;41(7):1213–6.
[42] Yang JQ, Yang JF, Kang JF, Liu KY, Han RQ, Kirsch P. Correlation between the dielectric traps and BTI characteristics of high-k/metal gate MOSFETs. In: IEEE trans electron devices int integ rel wrksp, Stanford Sierra, CA, 1930-8841, Oct; 2010.
[43] Kerber A, Cartier E, Pantisano L, Degraeve R, Kauerauf T, Kim Y, et al. Origin of the threshold voltage instability in SiO_2/HfO_2 dual layer gate dielectrics. IEEE Electron Device Lett 2003;24(2):87–9.



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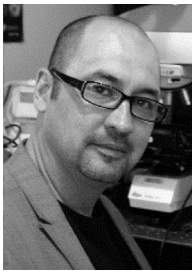

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